Thermal Cycle Reliability of PBGA/CCGA 717 I/Os

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Abstract

Status of thermal cycle test results for a nonfunctional daisy-chained peripheral ceramic column grid array (CCGA) and its plastic ball grid array (PBGA) version, both having 560 I/Os, were presented in last year's conference. Test results included environmental data for three different thermal cycle regimes (-55°/125°C, -55°/100°C, and -50° /75°C). Update information on these—especially failure type for assemblies with high and low solder volumes—were presented. The thermal cycle test procedure followed those recommended by IPC-9701 for tin-lead solder joint assemblies. Revision A of this specification covers guideline thermal cycle requirements for Pb-free solder joints. Some background information discussed during release of this specification with its current guideline recommendations were also presented.

In a recent reliability investigation a fully populated CCGA with 717 I/Os was also considered for assembly reliability evaluation. The functional package is a field-programmable gate array that has much higher processing power than its previous version. This new package is smaller in dimension, has no interposer, and has a thinner column wrapped with copper for reliability improvement. This paper will also present thermal cycle test results for this package assembly and its plastic version with 728 I/Os, both of which were exposed to three different cycle regimes. Two cycle profiles were those specified by IPC-9701A for tin-lead, i.e. -55 to 100°C and -55 to 125°C and one was a cycle profile specified by Mil-Std-883, i.e., -65°C /150°C which is generally used for ceramic hybrid packages. Per IPC-9701A, test vehicles were built using daisy chain packages and were continuously monitored. The effects of many process and assembly variables—including corner staking commonly used for improving resistance to mechanical loading such as drop and vibration loads—were also considered as part of the test matrix. Optical photomicrographs were taken at various thermal cycle intervals to document damage progress and behavior. Representative samples of these along with cross-sectional photomicrographs at higher magnification taken by scanning electron microscopy (SEM) to determine crack propagation and failure analyses for packages are also presented.

Key Words: Ceramic column grid array, CCGA, plastic ball grid array, PBGA, thermal cycle, staking, solder joint, inspection, conformal coat, corner staking

Introduction

Ball grid arrays (BGAs) and chip scale packages (CSPs) are now widely used for many electronic applications, including portable and telecommunication products. Systems-in-a-package (SIP) development is the most recent response to further ever increasing demand for integration of different functions into one unit to reduce size and cost and improve functionality. The SiP is now included in the iNEMI2005 roadmap stating that this technology "has rapidly evolved from specialty technology used in a very narrow set of markets to a broad market base, high volume technology that has a wide-ranging impact on the electronics market". The BGA version has now started to be extensively implemented for high reliability applications with generally more severe thermal and mechanical cycling requirements. The plastic BGA version of the area array package, introduced in the late 1980s and implemented with great caution in the early 1990s was further evolved in the mid 1990s to the CSP (also known as fine pitch BGA) having a much finer pitch from 0.4mm to 0.3mm. Because of these developments, it is becoming even more difficult to distinguish different array packages by size and pitch.

Extensive work has been carried out by the JPL Consortia in understanding technology implementation of area array packages for high reliability applications. This work (among other things) included process optimization, assembly reliability characterization, and the use of inspection tools, including X-ray and optical microscopy, for quality control and damage detection due to environmental exposures. Lessons learned by the JPL-led team and others have been continuously published [1-2].

The BGA package with 1.27 mm pitch has been the package of choice for commercial applications. However recently, a ceramic package version specifically tailored for high reliability applications was used to provide processing power required for the Spirit and Opportunity Mars Rovers built by NASA-JPL. Both Rovers successfully completed their 3-months mission requirements and continued exploring the Martian surface for many more moths, providing amazing new information on previous environmental conditions of Mars and strong evidence that water exists on Mars. It is important to note that the field

programmable gate array (FPGA) area array packages were kept in a benign warm electronic box (WEM) environment and the mission is considered to be relatively short. Electronics in a WEM are heated in order to avoid exposure to the extreme Martian weather that can reach as low as -130°C. Thermal cycling represents the on-off environmental condition for most electronic products and therefore is a key factor that defines assembly reliability.

Area arrays come in many different package styles. These include the plastic ball grid array (PBGA) with ball composition of eutectic Sn63Pb37 alloy or slight variations such as Sn60Pb40. The ceramic BGA package uses a higher melting ball (Pb90Sn10) with eutectic attachment to the die and board. The column grid array (CGA or CCGA) is similar to a BGA except that it uses column interconnects instead of balls. The lead-free CCGA uses a copper instead of high melting lead/tin column. The flip chip BGA (FCBGA) is similar to the BGA, except that a flip chip die rather than a wire bonded die is used.

Three array configurations are popular. These are a) full array; b) staggered array; and c) peripheral array. Plastic packages come in all styles, whereas ceramic package are generally limited to a full array configuration. Fully populated array packages presents some significant routing challenges if a conventional PWB with plated through-hole (PTH) vias are considered for the design. Peripheral plastic packages have been developed to reduce solder joint failures at the die edge as well as to improve routability characteristics. However, for ceramic packages there is a lesser need for a peripheral array because the CTE mismatch between die and package material is negligible. Hence, most ceramic packages are supplied in full array configuration including the CCGA717 I/Os used in this investigation. When the ceramic package pad pattern simulates its plastic package version, e.g. the CCGA 560 I/Os, the package might come in the form of peripheral array.

This paper will first present a summary of Sn-Pb solder volume on assembly reliability of CBGAs and CCGAs since optimum volumes for the two package types are shown to be different. It will then compare SEM photomicrographs of failures for Sn-Pb and Pb-free for CCGA assemblies after thermal cycling. Guidelines for Pb-free solder joint attachment were given in a recent Revision A of IPC-9701[8] that includes a recommendation for dwell times with consideration of thermal cycle efficiency and creep. This specification; however, does not include the background information and the discussion made during the development of this guideline requirement. Hence, a brief discussion with some background information on this topic will also be presented. Numerous test vehicles with two CCGA package styles and their counterparts plastic packages were assembled on printed wiring boards (PWB) and were subjected to thermal cycling and their failures established. Details on the design and assembly of experimental test vehicles (TVs) will also be summarized, including the following: PWB design and solder paste print efficiency using automatic and manual printing, reflow by vapor phase or rework station, corner staking adhesive and conformal coat will also be summarized. The TVs were subjected to four different thermal cycle regimes including -50° to 75°C. Representative cycles to failure, failure mechanisms, and cross-sectional photomicrographs for these packages under different thermal cycle regimes are also presented.

IPC Standard for Thermal Cycle Performance Requirement for SMT Assemblies

An industry-wide guideline document, IPC-SM-785 for accelerated reliability testing of solder attachments, *Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments*, has been in existence for more than a decade. Only recently has industry agreed to release an industry-wide specification, IPC-9701, in response to needs for implementation of BGA and CSP technology[8]. Although the IPC-SM-785 guidelines document remains very valuable and is still valid in terms of providing fundamental understanding, it sets no testing requirements and performance standards. As has been well established by industry and the JPL Consortia [1-5], many variables could be manipulated to either favor or disfavor test results. Considerable resources and time could be wasted to generate failure data not related to solder attachment. An example is the use of a surface finish having the potential of inducing interfacial rather than solder joint failure. This mishap is especially likely to occur by a novice user/supplier.

The IPC-9701 specification addresses how thermal expansion mismatch between the package and the PWB affects solder joint reliability. In order to be able to compare solder joint reliability for different package technologies, numerous materials and process parameters were specified including the following:

- Specifies 0.093 inch for PWB (e.g. FR-4) thickness in order to minimize bending and to achieve conservative values on cycles-to-failure data.
- Limits surface finish choices to OSP (organic solder preservative) and HASL(hot air solder level) in order to eliminate potential of interfacial failure
- Limits pad configuration to NSMD (non-solder mask defined or Cu defined) in order to eliminate failure due to stress riser.
- Defines PWB-pad size to be 80% to 100% of package-pad size in order to have a realistic failure

The newest revision, IPC-9701A has updated to include guidelines for Pb-free solder alloys. The appendix B of this specification provides guidelines for modifications required to IPC-9701 for Pb-free solder joints. Currently, there are only

limited data and insight to determine acceleration factors and acceleration models for lead-free [9-12]. Data on the impact of various thermal cycle profiles on the results of accelerated testing in comparison to eutectic tin-lead solder are still being gathered by industry.

Acceleration thermal cycle test results—especially when are compared to lead-free solder alloys—are sometimes inaccurately assumed to be the same as product reliability. Correlations between acceleration testing and product reliability for Sn-Pb have been more or less established during many years of investigation and product use. For the lesser understood Pb-free solder attachments, such correlations remain to be better established. Reliability is the ability of a product, here surface mount solder attachments, to function under given conditions and for a specified period of time without exceeding acceptable failure levels. Therefore, as the supposition that Pb-free solder joints are either more or less reliable than standard Sn-Pb solder joints is based only on unsubstantiated laboratory test results Such general statements are incomplete when either the Pb-free alloy composition or when product information and use conditions are not specified. It is emphasized that product reliability needs to be estimated for solder joints under relevant use conditions.

Modification of IPC-9701 to include requirement for Pb-free solder attachment was assumed to be an easy task at the start of the effort since abundant information on thermal cycling for Sn-Pb was already well established. However, it soon became apparent that even a trend cannot be established for acceleration thermal cycling data for Pb-free. The literature data are summarized by this author and plotted in Figure 1 as relative cycles to failure for Pb-free to Sn-Pb on the y axis and thermal cycle conditions on the x axis. Relative cycles to failures may be better (>1) or worse than Sn-Pb depending on package type, thermal cycle range, cycle profile, and dwell times at temperatures. For example, cycles to failures for Pb-free PBGA 256 I/Os (plastic ball grid array) assemblies are about twice those Sn-Pb, whereas for those of LCCC (leadless ceramic chip carrier) are about half of Sn-Pb respectively when subjected to accelerated thermal cycling in the range of -40° to 125°C. Temperature range and dwell time also affect relative accelerated failure cycles as apparent from test data generated for CBGA 625 I/Os from 0° to 100°C and -40° to 125°C.

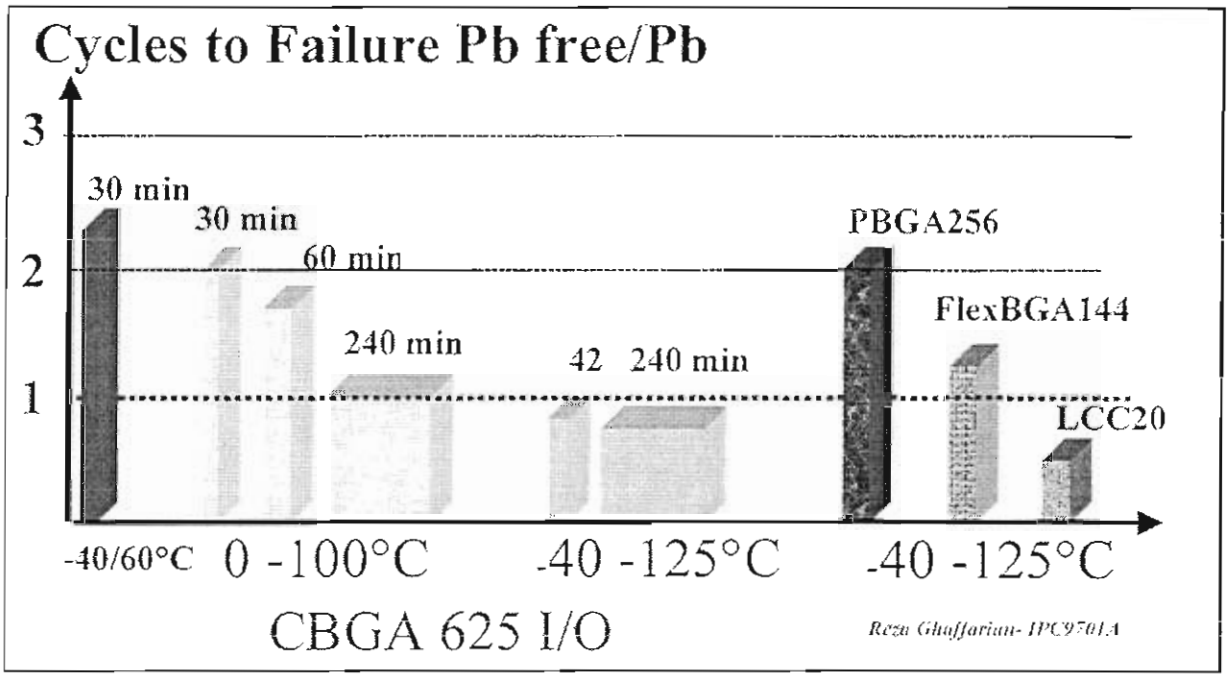

Figure 1 Cycles-to-failures for SAC (Sn-Ag-Cu) solder attachment dependence on thermal cycle range and state of stress/strain (data from different sources including [12]).

Various authors have attempted to theoretically explain the apparent contradiction of accelerated test results–projection can be made by using creep hysteresis loops (energy) as the baseline for modeling. The effect of dwell time depends on the temperature range and the maximum temperature. Such effects can be low to high as predicted by modeling. Dr. Jean-Paul Clech has shown theoretically in Reference 11 that the most efficient dwell times at 100°C (0°-100°C cycle) are 10 minutes for tin-silver-copper (SAC) and 3-4 minutes for Sn-Pb solder joints, respectively. Based on very limited test data and contrary to conventional understanding, he also postulates that thermal cycling at higher mean temperature may show improved cycles to failures when compared to a lower mean temperature.

Extensive discussions were made among the IPC-9701 committee team members as how best to capture the apparent conflicting accelerated test data and generate them into requirements. Initially, a large number of figures representative of such conflicting test results were included in the Appendix B of IPC-9701A to show different team members' points of view for specifying the dwell time requirements. However, based on comments received after its wider distribution to industry, these figures were removed from this specification and will be published at the APEX 2006 conference sponsored by IPC. In addition, the Appendix B of IPC-9701A title was changed to "*guideline*" rather than "requirement" since no industry-wide agreement could be reached on even the definition of thermal cycle profile. Based on numerous discussions within the last two years, two thermal cycle profiles were recommended for (SAC) solder attachments depending on the reliability approach and use conditions. These are:

- Condition D10 (10 minute dwell), requiring 10-minute dwells at the hot/cold temperature extremes. This is possibly the most efficient accelerated thermal cycle profile since it induces the most strain energy per unit of time (considering the entire cycle) or per unit dwell time. Cycles-to-failure data generated under this condition should generally be used as stand-alone only and only when damage accumulation is understood by modeling. The test results could be used for comparison to those of lead-based solder assemblies to show theoretically whether their performance is better or worse.
- Condition D30^{+} (30 minutes or higher dwell), requiring dwells of 30 minutes and higher (60 minutes) at the hot/cold temperature extremes in order experimentally to induce creep damage somewhat comparable to lead-based solder. Modeling in conjunction with experimental data at different dwell times may be required to better define such a comparison.

An OSP surface is recommended for the Pb-free base solder alloys even though the final version may include immersion silver (IAg) based on additional inputs. For Sn-Pb, the acceptable surface finish was HASL. HASL is not allowed for a lead-based alloy since it is not compatible with lead-free solder interconnections. Other surface finishes can be used for the manufacturer's internal data comparison. Electoless nickel/immersion gold (ENIG) surface finish also can be used for internal data comparison; however, there is a risk of introducing unintended immature failure as documented by industry. In this specification, the thermal cycle (TC) test ranges, test profile, and the number of test cycles (NTC) reported were also standardized. These include the reference cycle in the range from 0° to 100°C (TC1) and the severe military cycle condition from –55° to 125°C (TC4). Three out of five total TC conditions are identical to the test conditions recommended by JEDEC 22 Method A104, Revision A. The NTCs varied from a minimum value of 200 cycles to a reference value of 6000 cycles.

Tin-lead and Pb-free solders with Ceramic Column Grid Array (CCGA)

Figure 2 shows SEM photomicrographs and cross-sections of the 560 CCGA assemblies after cracking due to thermal cycling. Figure 3 shows the microstructure of another CCGA package assembled with lead-free (Sn/Ag/Cu) solder paste[13]. For CCGA assemblies, the 3D optical microscopy and visual inspection are limited to inspection of the outer rows. Such inspection can be performed only when sufficient gaps are allowed between the assembled parts. Note that the assemblies show signs of damage/cracking after thermal cycling.

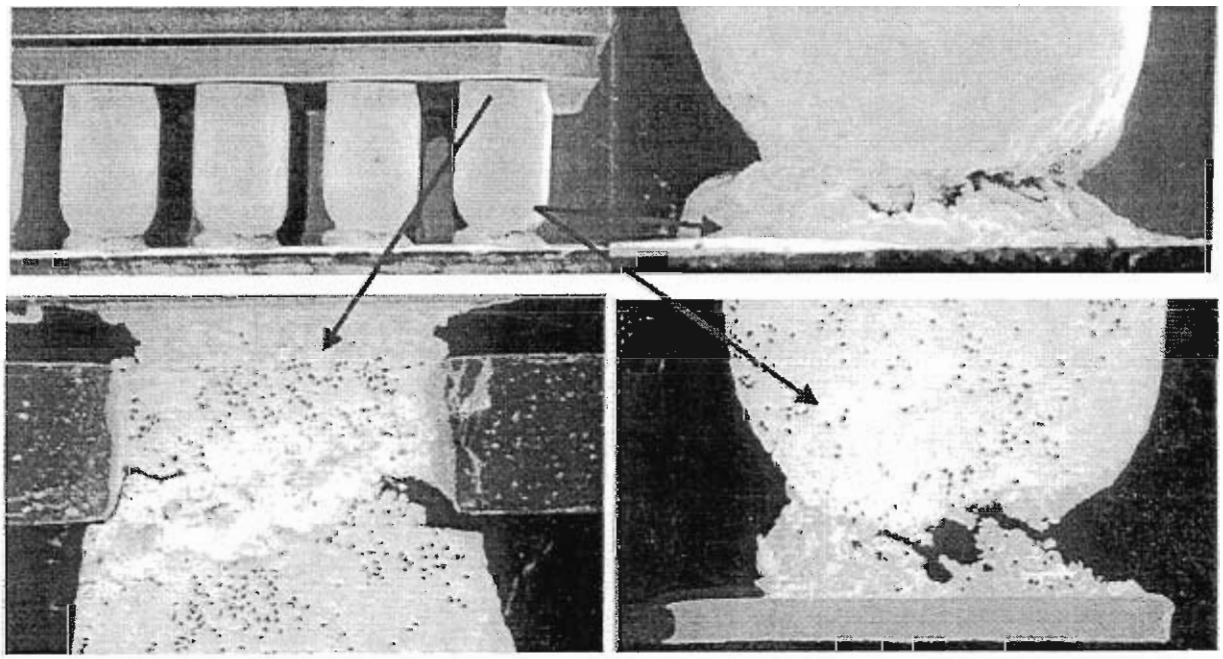

Figure 2 SEM photomicrographs and cross-sections of CCGA560 I/O assembled with tin-lead solder after thermal cycling showing damage/cracks

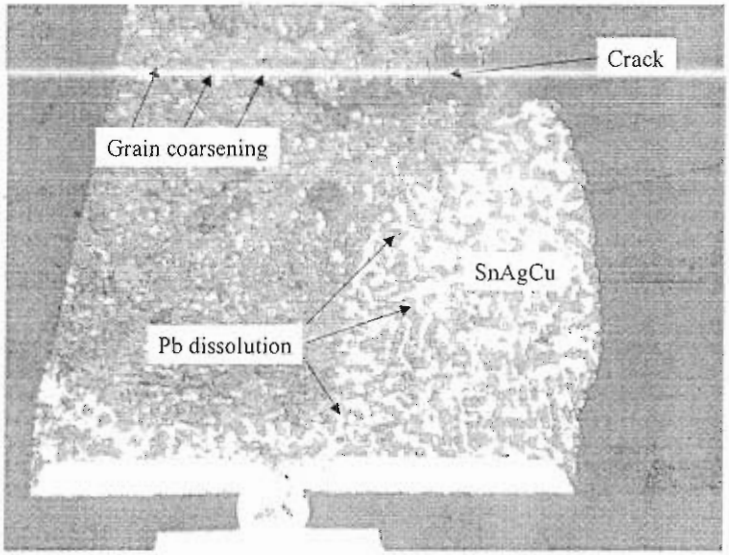

Figure 3 1657 I/O CCGA high-lead solder column on a microvia pad PWB with Sn-Ag-Cu solder joints (Courtesy of Dr. D. Shangguan/T. Castello)

Effect of Solder Joint Volume on CCGA Assembly Reliability

In a previous paper[14] cycles to failure were tabulated for a number of CCGAs/CBGAs with different configurations selected from very limited data reported in the literature. Data were chosen to illustrate the effects of a few key parameters on reliability including the effect of the thermal cycle range, package size and materials, die size, and PWB thickness. Contrary to PBGAs, CCGAs/CBGAs assembly reliability is significantly affected by the amount of solder volume. Solder volume is the most important key process variable affecting the reliability of CCGAs/CBGAs. Recommended minimum, optimum and maximum solder paste volumes for both CBGA and CCGAs are shown in Table 1 [15,16]. The effect of solder volume for CBGAs is intuitive since higher solder volume increases the solder balls' stand-off height, but this is not the case for the CCGA assemblies where column flexibility also plays role on reliability.

For CBGAs, it has been shown that increasing solder-paste volume increases reliability, but only to a point. When the paste volume passes 10,000 cubic mils (0.16 cubic mm), the reliability no longer increases because the solder paste has filled the area between the ball and the card. Additional solder paste moves up the ball toward the module, making the ball look like a column. When the fillet dimension at the card surface is maximized, so is the reliability.

This trend may not be true for at least one type of CCGA package with 1.27 mm pitch. Unlike the CBGA product, high solder paste volume can actually start to decrease the interconnection reliability. As the volume increases, so does the fillet height on the column. This increased fillet height reduces the effective length of the flexible column, thus making it stiffer. This effect—while true for both cast and wire—is more pronounced for the cast because it is stiffer in nature due to its larger diameter [16]. In a comprehensive investigation performed for this category of packages, it has been shown that assemblies with a minimum acceptable solder paste showed slightly higher reliability than those with nominal and much better than those with higher solder volume. To avoid inducing opens however, the use the nominal rather than minimum solder paste volume is recommended.

Table 1 Solder paste recommendation for CBGA and CCGA, 1.27 mm pitch

Solder volume	Minimum Paste mil^3 (mm^3)	Optimal Paste mil^3 (mm^3)	Maximum Paste mil^3 (mm^3)
CBGA	4800 (0.089)	6500-7500 (0.10-0.120)	10000 (0.160)
CCGA	3000 (0.0470)	5000-5600 (0.078-0.088)	7600 (0.120)

Objectives

The purpose of this investigation was to characterize the reliability of area array packages with 560, 717, and 728 I/Os. Preliminary results of the 560 I/O 2nd level package assemblies were previously given in the IEEE CPMT[14]. These included the

effect of corner staking and the thermal cycle range on failure of ceramic column grid array and its plastic counterparts with the same peripheral package configuration. An additional discussion of first failure for low and high solder volumes is discussed in this paper.

The new version of this field programmable gate array package with higher processing power is smaller in dimension and of less weight. These packages are fully populated with 728 I/Os in the plastic configuration and 717 I/Os in the ceramic column grid array (CCGA) package (see Figure 4). For the CCGA 717, the 3-corner solder columns from package corners have been removed by the package manufacturer to improve reliability (Figure 5). Comparing this Figure to Figure 1 for the CCGA 560 I/O package, it is evident that the columns for the CCGA 717 I/Os are thinner and present different features. For this reason, assembly processing parameters are different from the 560 I/O package and need to be optimized prior to establishing their 2nd level solder joint reliability.

A design of experiment (DOE) was utilized to cover processing as well as other aspects that are considered to be unique for the potential use of these packages for high reliability applications. Solder joint reliability is affected by many variables including solder volume. The following parameters were either characterized or evaluated as part of the DOE implementation.

- Designed two pad sizes, one for the CCGA 560 I/Os and smaller pads for the PBGA attachment. PBGAs were assembled on both pad sizes to evaluate PBGA interchangeability with the CCGA.
- Assembled CCGA 717 I/Os and 728 I/Os on one pad that considered to be acceptable for the CCGA 717 I/Os. PBGA corner balls were removed in the PBGA 728 assembly to utilize the 717 I/O pad pattern (see Figure 4).
- Utilized four different stencil designs, a relatively thicker mini-stencil up to 10.5 mil thick especially designed for the CCGA 560, an 8 mil thick stencil designed for the CCGA 717 I/Os, and a standard 6 mil thick stencil to assemble PBGAs and other surface mount packages. Solder paste print volumes were significantly varied depending on package types, stencil design, and paste printing process.
- Included CCGA and PBGA assemblies with added corner staking adhesive and conformal coat. Corner-staking adhesive bonds are generally used to enhance resistance to mechanical shock and vibration loads and conformal coat to protect solder joints from contamination including shorts due to conductive particulates.
- Packages were assembled in a vapor phase reflow machine or individually assembled using a rework station in order to establish differences in reliability between the two techniques. A rework station is an option for assembly in a high reliability manufacturing when only a few systems are being built, this is not an option for high volume manufacturing.

The assemblies were subjected to four types of thermal cycles. The process and results for reliability of CCGA package assemblies are discussed below and compared to their PBGA counterparts.

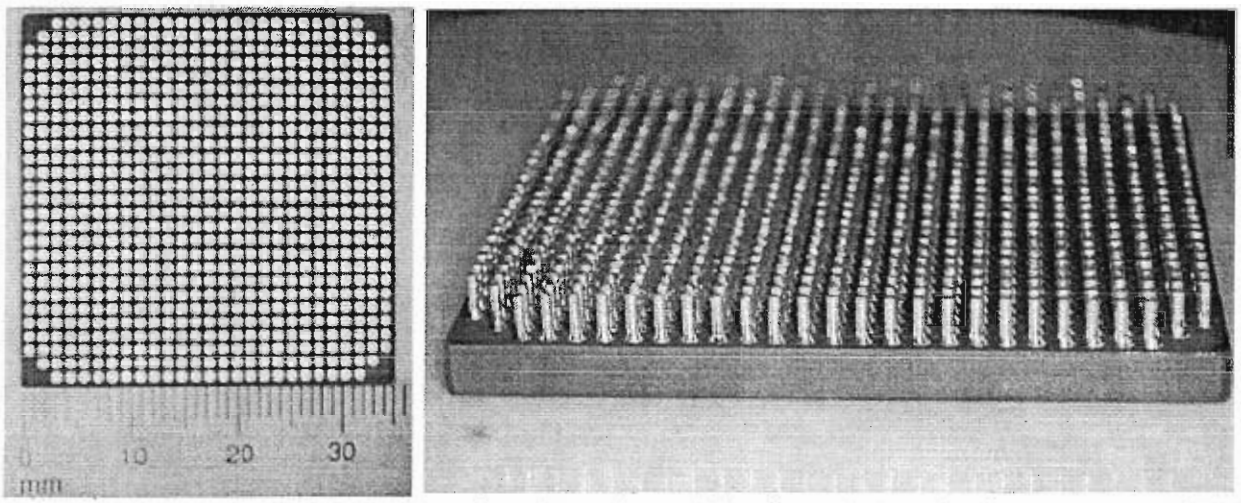

Figure 4 Photomicrograph of CCGA 717 I/O package dimension and its column feature showing no corner columns for reliability improvement

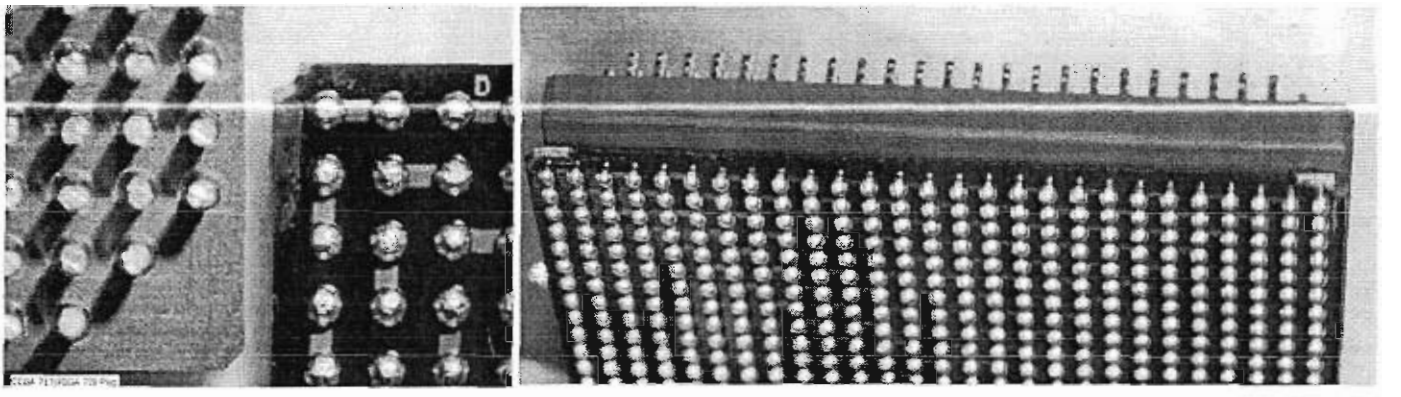

Figure 5 Photomicrograph of CCGA 717 I/O and its plastic counterparts with corner balls—corner balls removed in order to assemble the PBGA package on the CCGA PWB pad design

Test Vehicles

For the CCGA/PBGA 560 I/Os, a polyimide PWB was designed to accommodate two pad configurations, one configuration for the PBGAs and the other for the CCGAs. The pad sizes for the PBGA and CCGA were 24 and 33 mils, respectively. They pads were connected through their 24 mil diameter plated-through-hole vias (PTHV). Specific pairs of PWB pads were designed so that their connections within a package pair after assembly completed daisy chain patterns. Four key daisy chains for each package were used for continuous monitoring during thermal cycling. Four additional pads were added at each side of the package for manual probing and failure identification. For the CCGA 717 I/O and PBGA 728 I/Os, a high temperature FR-4 PWB with 0.091 inch thickness as specified by IPC-9701A with 32 mil pads connected to through hole vias was used. Figure 6 shows an assembled test vehicle having both CCGA 717 I/O and PBGA 728 I/O packages. Note the input and output traces that extend to the board edge and also the probing pads at the package peripheral for manually detecting failures.

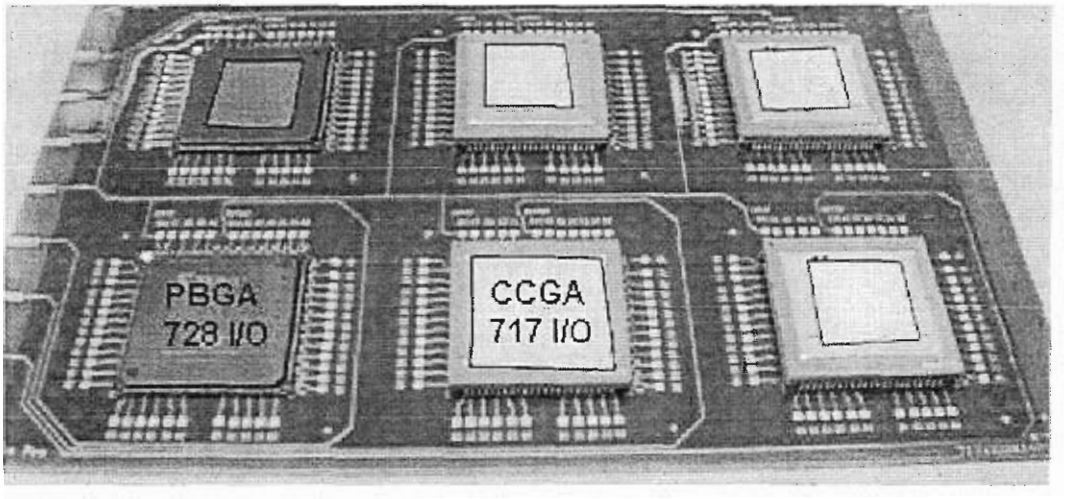

Figure 6 PWB design showing design-chained CCGA and PBGA packages, probing pads, and via daisy chains

The PWB pads had HASL surface finish. HASL and OSP surface finishes are specified in IPC-9701A as the recommended surface finishes for solder attachment reliability evaluation of tin-lead solder alloy. This is to avoid potential immature intermetallic failures such as those occasionally observed for the Au/Ni surface finish. Currently, only the OSP surface finish is recommended for lead-free solder alloys.

Stencil Design, Paste Print, and Volume Measurement

Table 2 lists estimated solder paste volumes achievable with different stencil thicknesses and aperture openings. The 6 and 7 mil stencil thicknesses represent the general stencil that could be used for paste application on PBGA and CCGA pad patterns, respectively. The mini-stencil with 8 and 10.5 mil thicknesses were used only for the manual paste print application for CCGA in order to achieve the higher paste volume recommended by the package supplier. In one case, a step down stencil design, from 8 mil to 6 mil thickness, was used to accommodate quality assembly of both the CCGA and the other finer pitch standard surface

mount packages. For this case, numerous conventional packages in the vicinity of CCGA had to be hand soldered since they were masked during automatic paste printing. The CCGAs were assembled in two facilities, each using their approved RMA paste and assembly process prodedures.

Table 2 Stencil parameters and solder volumes

Solder volume	Solder volume (mil^3)	Stencil Type
BGA 560 I/O-Aperture 23 mil-dia stencil 7mil	2909	Stencil
CCGA 560-Aperture 32 mil dia- stencil 7 mil	5632	Stencil
CCGA 560- Aperture 32 mil dia- Stencil 8 mil	6430	Stencil
CCGA 560-Aperture 32 mil dia- stencil 10.5 mil	8440	Mini-stencil
PBGA 728- Aperture 6 mil dia- Stencil 28 mil	4823	Mini-stencil
CCGA 717-Aperture 32 mil dia- stencil 8 mil	6430	Mini-stencil

Two RMA pastes at two facilities, Type III (-325+500) mesh, were used for paste printing using automatic and normal manufacturing parameters. Manual paste printing was performed when the mini-stencil was used. Each paste print on the PWB was visually inspected after printing for gross defects such as bridging or insufficient paste. Paste print quality was improved by adding paste when insufficient paste was detected, and solder paste was removed when bridging was discovered. Special attention was given for the inspection of corner pads. Solder paste heights were measured using a two different laser profilometers and an optical microscope with 3D dimensional measurement capability. Measurement was carried out at numerous locations that included corner and peripheral center pads in order to accumulate solder volume data and their distributions.

An example of laser measurement for the top left corner and solder paste distribution values is shown in Figure 7. The specific tool provides automatic control for measurement and the maximum level cut-off value. These specific features make it very difficult to expand the measurement to larger values. This led on many occasion to wrong readings due to an abrupt paste print. Eventually, the print height had to be verified through filler gages and the uniformity of solder paste print inspected by microscope. On the other hand, the 3D optical microscopy could reveal the distribution covering a larger area, but lacked accuracy (see Figure 8).

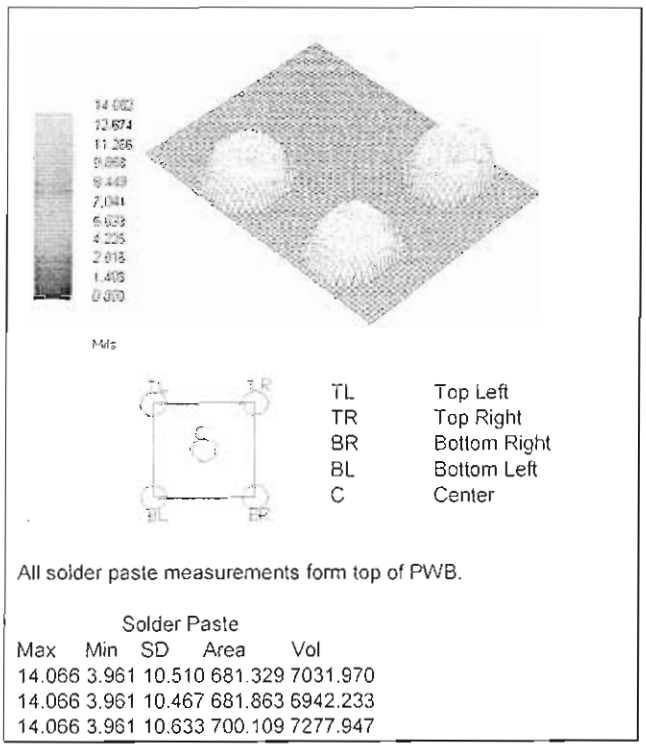

Figure 7 Solder paste distribution using a laser profilometer showing calculated paste volume

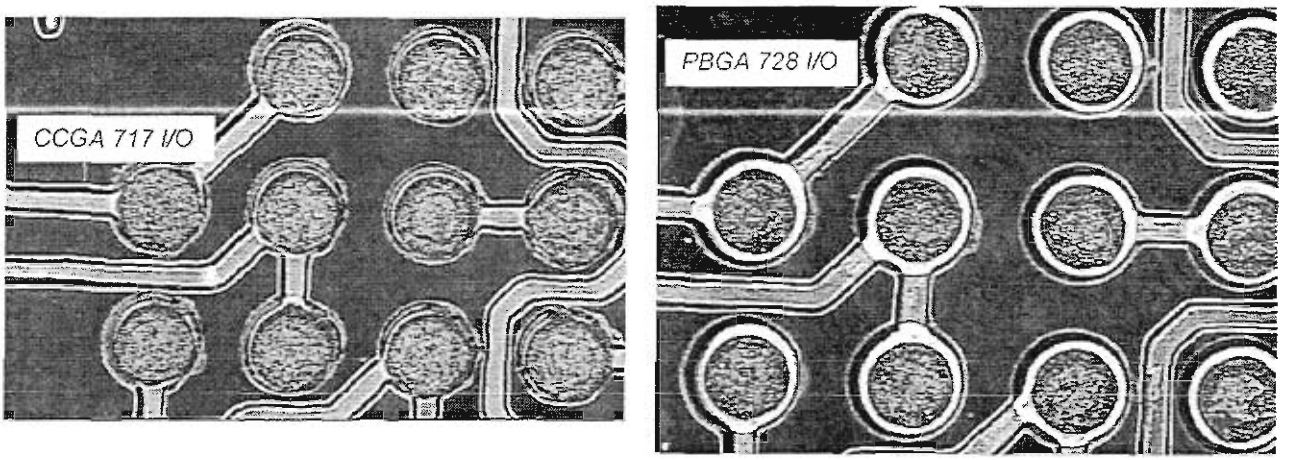

Figure 7 Solder paste deposition for CCGA 717 and PBGA 728 using the pad design for CCGA 717 I/O; higher solder paste volume required for CCGA package assembly in order to achieve optimum reliability

Test Results

Inspection before Environmental Tests

For high reliability electronic applications, visual inspection is traditionally performed by Quality Assurance personnel at various levels of the packaging and assembly, i.e., mandatory inspection points (MIPs). Solder joints are inspected and accepted or rejected based on specific sets of criteria. Further assurance is gained by subsequent short-time environmental exposure, by thermal cycling, vibration, and mechanical shock, and so forth. These screening tests also allow detection of anomalies due to workmanship defects or design flaws at the system level. For space application, generally 100% visual inspection is performed at prepackage prior to its closure (precap) and after assembly prior to shipment.

Visual inspection is somewhat useful for the area array packages, but obviously is of no value for hidden balls and columns under the package. X-ray inspection is needed for area array packages. However, in the case of CCGAs, the hidden solder joints could not be distinguished because of the heavy ceramic lid that inhibited X-ray penetration[6]. Visual inspection has a higher value for CBGA and CCGA assemblies since generally the solder fails at the exposed corners or periphery ball attachments. Peripheral balls and columns were inspected visually using an optical microscope at the start and during thermal cycling to document damage progress. Figure 9 shows photomicrographs of solder joints of CCGA 717 assemblies prior to thermal cycling. Note good solder joints with smooth surface adjacent to a joint with ridged solder. Minor modification in reflow steps did not remove this evenness.

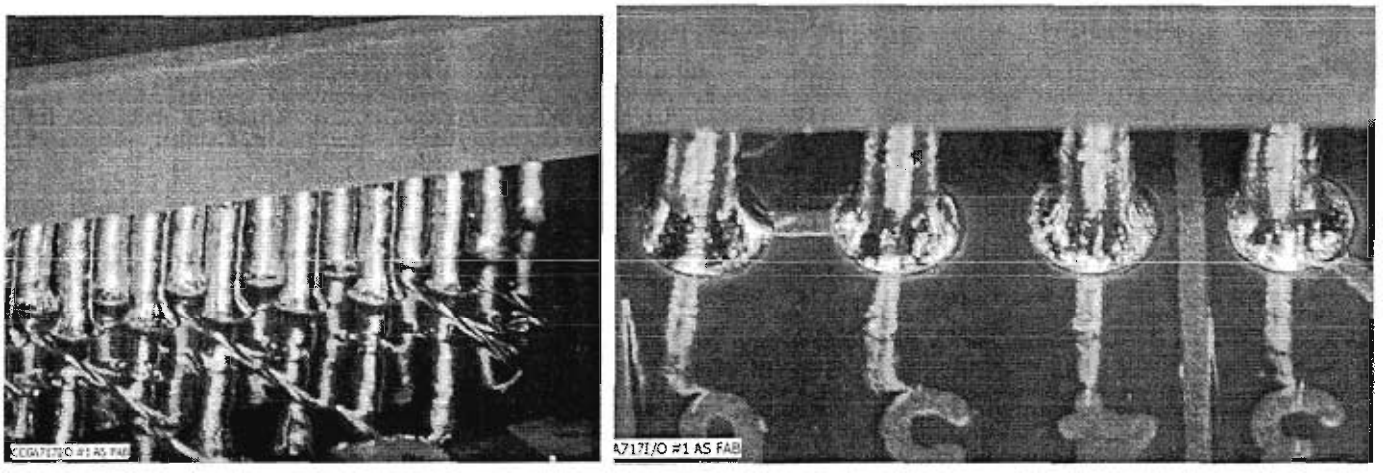

Figure 9 Optical photomicrographs of a PBGA and a CCGA after assembly

Thermal Cycle Test Profile

Four different thermal cycle profiles were used with the following thermal profiles. These are:

- Cycle A: The cycle A condition ranges from –50° to 75°C with a 2° to 5°C/min heating/cooling rate. Dwells at extreme temperatures are at least 10 minutes with a duration of 105 minutes for each cycle.

- Cycle B: The cycle B condition ranges from –55°to 100°C with a 2° to 5°C/min heating/cooling rate. Dwells at extreme temperatures are 15 minutes .
- Cycle C: The cycle C condition ranges from –55° to 125°C with a 2° to 5°C/min heating/cooling rate. Dwells at extreme temperatures are at least 10 minutes with a duration of 159 minutes for each cycle.
- Cycle D: The cycle D condition ranges from –65° to 150°C with about a 20°C/min heating/cooling rate. Dwells at extreme temperatures are at least 10 minutes with a duration of about one hour for each cycle.

The criteria for an open solder joint specified in IPC-9701A were used as guidelines to interpret electrical interruptions. Generally, once the first interruption was observed, many additional interruptions within 10% of the cycle life also occurred. This was especially true for the ceramic packages. Opens were manually verified after removal from the chamber at the earliest convenient time.

Test Results after Thermal Cycles

CCGA 560 I/O Failure Characterizations by Optical Microscopy

Figure 10 shows optical photomicrographs of both PBGA and CCGA 560 I/O assemblies after 991 A condition (-50°/75°C) thermal cycles even though no failure was yet observed. The CCGA solder joints showed some signs of damage. This is not significant if only solder interconnect to the board is considered. Figure 11 shows the first failure occurrence for the CCGA assembly with high solder volume detected by continuous monitoring at 1,075 cycles and removed at 1,138 cycles for inspection and failure verification. It is interesting to note that failure did not occur at the package site; therefore, solder joint damage at board interface may not always be used as a representative of damage progress. In addition, solder joint failure is not at the corner columns as expected. Solder joint damage conditions for assemblies with low and high solder volume are shown in Figure 12– significant damage at the board site for the low solder volume condition. Failures were in solder joints at the board site for the assembly with low solder volume as shown in Figure 13 taken at 1459 thermal cycles. For corner columns, note that the columns are tilted toward the center of the package.

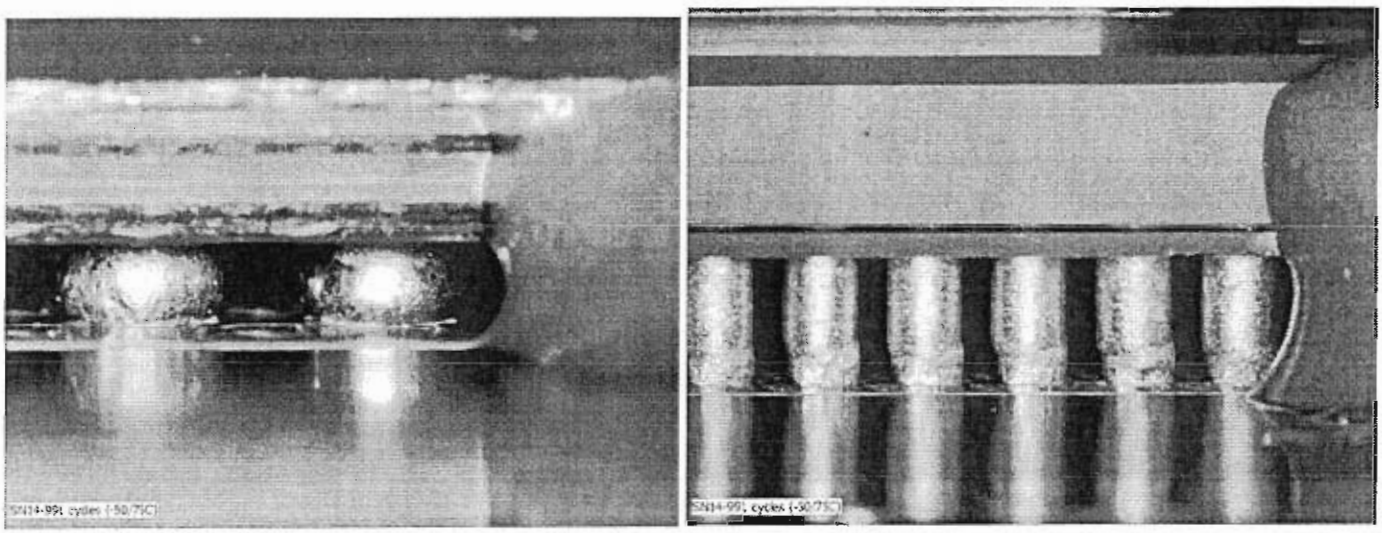

Figure 10 Optical photomicrographs of PBGA (left) and CCGA built with 105 mil thick stencil after 991 cycles (-50/75°C); corner staking adhesives are apparent at the two corners

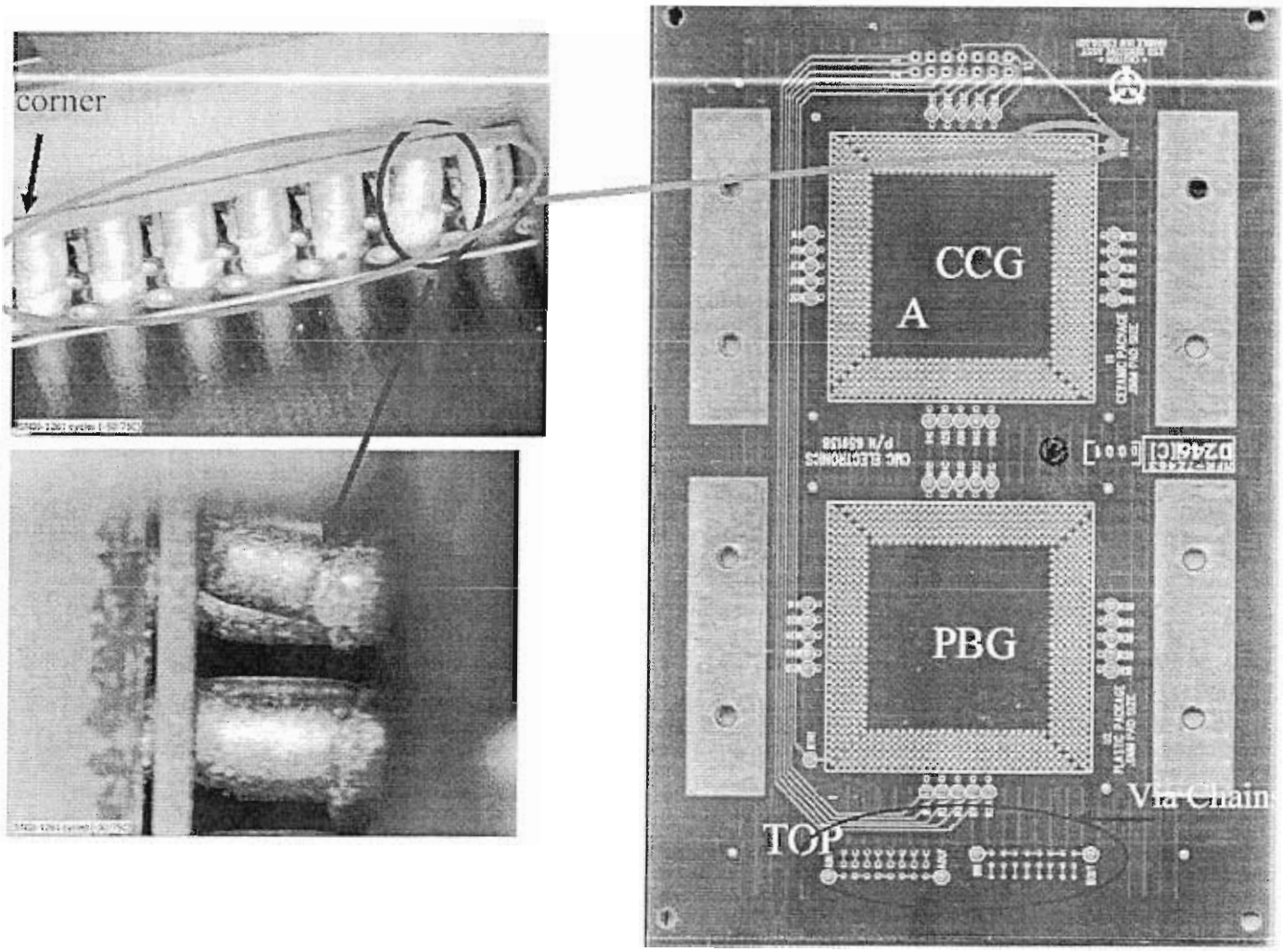

Figure 11 Optical photomicrographs of CCGA built with 10.5 mil thick stencil after 1138 cycles (-50°/75°C) with cracking from the package site rather than the board site commonly occurring

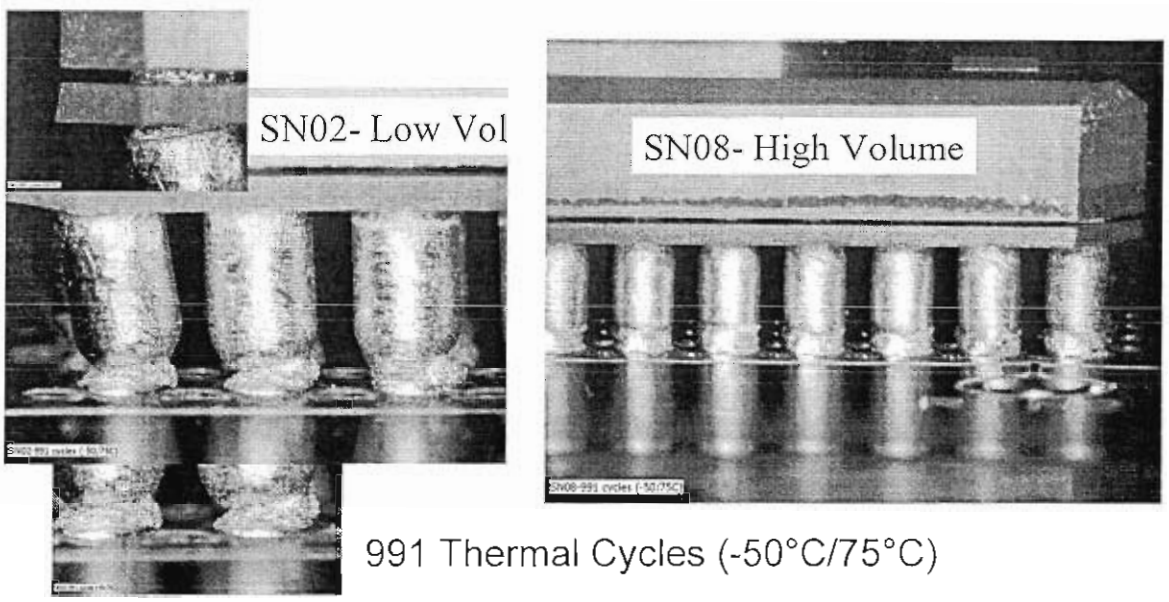

Figure 12 Optical photomicrographs of CCGA assemblies built with 8 mil (left) 105 mil thick stencils after 991 cycles (-50°/75°C)

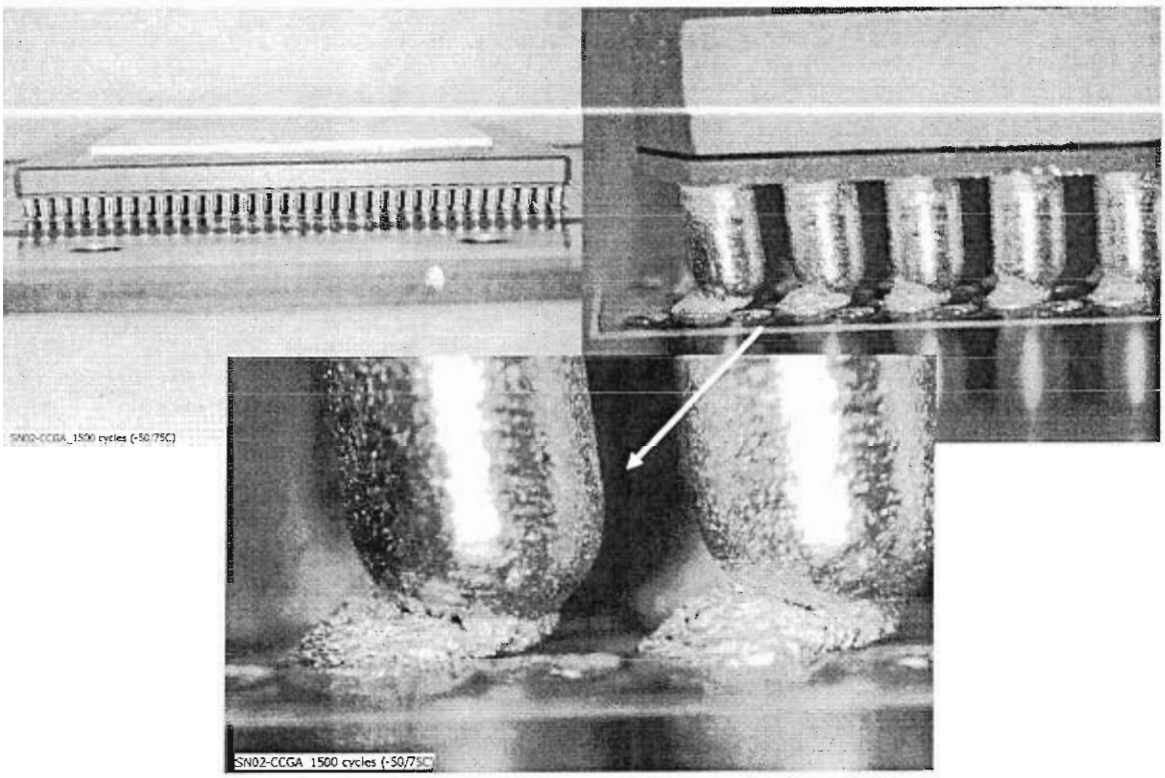

Figure 13 Optical photomicrographs of CCGA built with 8 mil thick stencil after 1459 cycles (-50°/75°C) with cracks in solder joints at the board site and shift of the corner columns towards the package center

CCGA 717 I/O Failure Characterizations by Optical Microscopy

Figure 14 shows optical and SEM photomicrographs of two CGA 717 I/O assemblies at 200 and 500 thermal cycles (-55°/100°C). The solder joints show some signs of minor damage. Optical photomicrographs for a CCGA package assembly with corner and without corner staking adhesive after 950 thermal cycles are shown in Figure 15. It appears that damage has not significantly increased; it is more severe for the one with corner staking. SEM photomicrographs for different columns after 950 cycles are shown in Figure 16. Even though no failures were yet detected by electrical monitoring, signs of damage at the board and package sites are apparent.

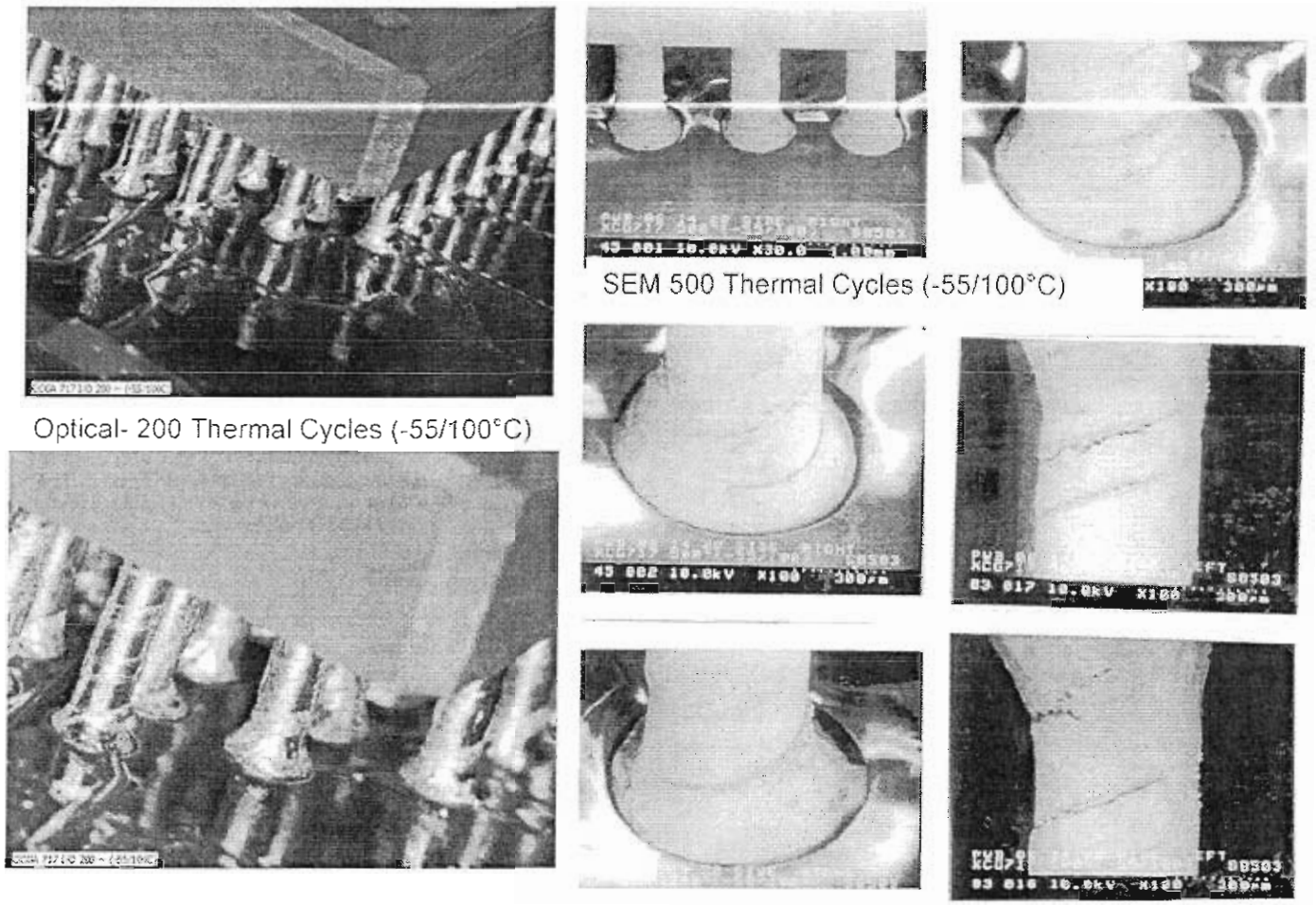

Figure 14 Optical photomicrographs of CCGA a 717 I/O assembly (left) at 200 and SEM photomicrographs at 500 thermal cycles (-55°/100°C) showing some signs of damage at 500 cycles is apparent

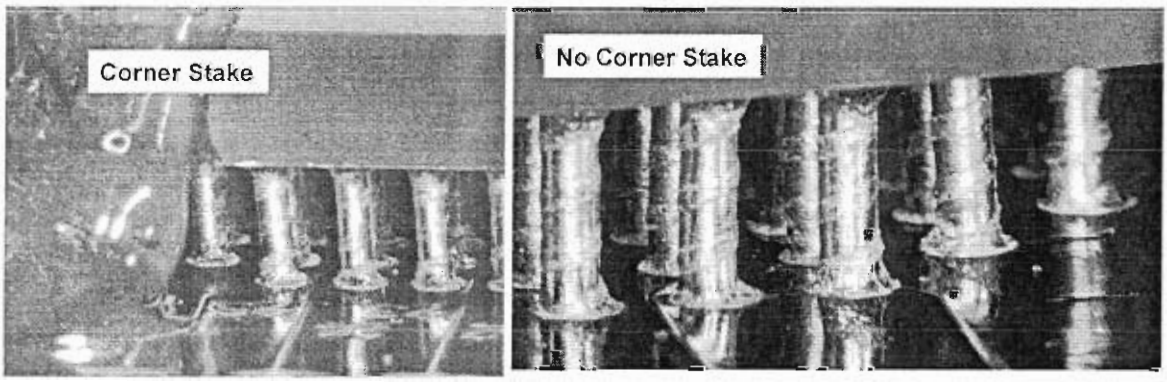

Figure 15 Optical photomicrographs of two CCGA 717 I/O assemblies with (left) and without corner stake at 950 thermal cycles (-55°/100°C) with a minor crack at the corner column with corner staking

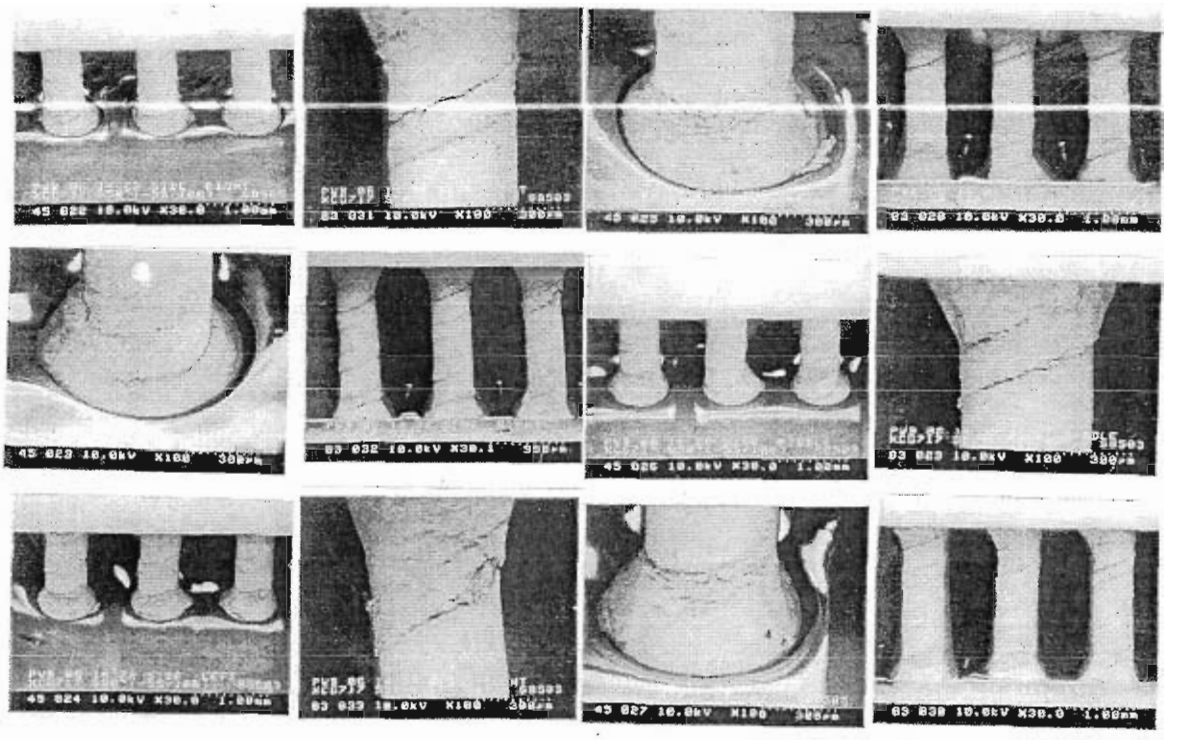

Figure 16 SEM photomicrographs of CCGA 717 I/O assembly at 950 thermal cycles (-55°/100°C) showing signs of microcracking

Conclusions

It is well established that solder joint reliability of plastic packages on polymeric boards is typically better than that of their ceramic counterparts. This trend was verified during our investigation. The current status of thermal cycles for the two CCGA package assemblies is as follows:

- Plastic package assemblies did not show failures to 2000 cycles whereas CCGA 560 I/O assemblies showed the first failure at 1,075 cycles when they were subjected to –50°/75°C cycle. The first failure was from the package site since a relatively high solder paste amount was used for assembly. For a lower solder volume, failures occurred at the board site.
- None of the PBGA 728 I/O and CCGA 717 I/O assemblies failed during continuous monitoring when subjected to 950 thermal cycles in the range of –55° to 100°C. These include those assembled with either vapor phase reflow or the rework station and assemblies with and without corner staking as well as those conformally coated. Visual inspection and manual probing was performed at numerous intervals and revealed no signs of opens, further verifying continuous monitoring test results.
- None of the PBGA 728 I/O and CCGA 717 I/O assemblies failed during continuous monitoring when subjected to 200 thermal cycles in the range of –55° to 125°C. Only those with and without corner staking adhesive test vehicles were tested.
- No failure was noted in the case of the two CCGA 717 I/O assemblies which were subjected to 100 thermal cycles in the range of –65° to 150°C.
- The CCGA 717 I/O assemblies showed various levels of solder joint damage at 950 cycles (–55°/100°C) when inspected optically and by SEM. For those with corner staking adhesive, the corner columns showed a higher damage level compared to their counterparts without staking.

It is difficult to identify damage levels for PBGA assemblies; therefore, at a later stage of thermal cycling both PBGA and CCGA assemblies will be subject to dye-and-pry and cross-sectioning to better characterize damage type and level.

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